CLAIMS

1. A system comprising:

a plurality of cores;

a first test access port controller coupled to at least one core;

a second test access port controller coupled to at least one core; and

a select pin to control the first and second test access port controller to support a plurality of system modes of operation.

2. The system of claim 1 further comprising:

a first multiplexer coupled to the first test access port controller, the second test access port controller, and to a first plurality of Joint Test Action Group (JTAG) signals; and

a second multiplexer coupled to the second test access port controller, a second plurality of Joint Test Action Group signals and to a plurality of pins.

3. The system of claim 1 wherein the system is a system on a chip (SoC).

4. The system of claim 1 wherein the plurality of system modes of operation is at least two of a debug mode, an emulation mode, or a test of at least one of the plurality of cores.

5. The system of claim 2 wherein the second multiplexer forwards the plurality of JTAG signals to the second test access port controller for either a debug mode of operation or an emulation mode of operation.

6. The system of claim 2 wherein the first multiplexer forwards the plurality of JTAG signals to the first test access port controller for either a debug mode of operation, or an emulation mode of operation, or to test one of the cores.

7. The system of claim 2 wherein the second multiplexer does not forward the plurality of JTAG signals to the second test access port controller for the system mode of operation to test one of the plurality of cores, and the plurality of pins coupled to the second multiplexer are utilized for other functional purposes for the system mode of operation to test one of the plurality of cores.

8. A method for controlling test access port controllers comprising:

generating a select signal;

selecting either a first test access port controller or second access port controller for a first mode of operation in response to the select signal; and

selecting both the first test access port controller and second access port controller for a second mode of operation in response to the select signal.

9. The method of claim 8 further comprising:

multiplexing between a plurality of Joint Test Action Group signals and a plurality of pins.

10. The method of claim 8 wherein the select signal comprises either a single pin or a combination of two pins.

11. The method of claim 8 wherein the first mode of operation is testing a single core.

12. The method of claim 8 wherein the second mode of operation is either a debug mode of operation or an emulation mode of operation.

13. The method of claim 9 wherein the multiplexing comprises:

forwarding the Joint Test Action Group signals in response to the second mode of operation; and

forwarding the pins in response to the first mode of operation for other functional uses.

14. A system comprising:

a plurality of cores;

a first multiplexer coupled to a first test access port controller and to at least one core;

a second multiplexer coupled to a second test access port controller and to at least one core;

a first pin to control the first multiplexer; and

a second pin to control the second multiplexer.

15. The system of claim 14 further comprising:

a plurality of Joint Test Action Group signals coupled to the first and second multiplexer; and

a plurality of pins coupled to the second multiplexer.

16. The system of claim 14 wherein the first pin is to select a core for a test mode of operation.

17. The system of claim 14 wherein the second pin is to select either one of a functional mode of operation, or a debug mode of operation, or an emulation mode of operation.

18. The system of claim 15 wherein the second multiplexer forwards the plurality of JTAG signals to the second test access port controller for either a debug mode of operation or an emulation mode of operation.

19. The system of claim 15 wherein the first multiplexer forwards the plurality of JTAG signals to the first test access port controller for either a debug mode of operation, or an emulation mode of operation, or to test one of the cores.

20. The system of claim 14 wherein the second multiplexer does not forward the plurality of JTAG signals to the second test access port controller for a mode of operation to test one of the plurality of cores, and the plurality of pins coupled to the second multiplexer are utilized for other functional purposes for the system mode of operation to test one of the plurality of cores.